INTEGRATED CIRCUITS

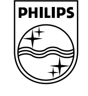
DATA SHEET

TDA2595
Horizontal combination

Product specification
File under Integrated Circuits, IC02

March 1987

Philips
Semiconductors





GENERAL DESCRIPTION

The TDA2595 is a monolithic integrated circuit intended for use in colour television receivers.

Features

- Positive video input; capacitively coupled (source impedance < 200 Ω)
- Adaptive sync separator; slicing level at 50% of sync amplitude
- Internal vertical pulse separator with double slope integrator
- Output stage for vertical sync pulse or composite sync depending on the load; both are switched off at muting
- φ_1 phase control between horizontal sync and oscillator
- Coincidence detector φ_3 for automatic time-constant switching; overruled by the VCR switch
- Time-constant switch between two external time-constants or loop-gain; both controlled by the coincidence detector φ3
- φ_1 gating pulse controlled by coincidence detector φ_3
- Mute circuit depending on TV transmitter identification
- φ_2 phase control between line flyback and oscillator; the slicing levels for φ_2 control and horizontal blanking can be set separately
- Burst keying and horizontal blanking pulse generation, in combination with clamping of the vertical blanking pulse (three-level sandcastle)
- Horizontal drive output with constant duty cycle inhibited by the protection circuit or the supply voltage sensor
- Detector for too low supply voltage
- Protection circuit for switching off the horizontal drive output continuously if the input voltage is below 4 V or higher than 8 V
- Line flyback control causing the horizontal blanking level at the sandcastle output continuously in case of a missing flyback pulse
- Spot-suppressor controlled by the line flyback control

QUICK REFERENCE DATA

Supply voltage (pin 15)	$V_{15-5} = V_P$	typ.	12	V
Sync pulse amplitude (positive video)	$V_{i(p-p)}$	min.	50	mV
Horizontal output current	I_4	typ.	50	mA

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102); SOT102-1; 1997 January 07.

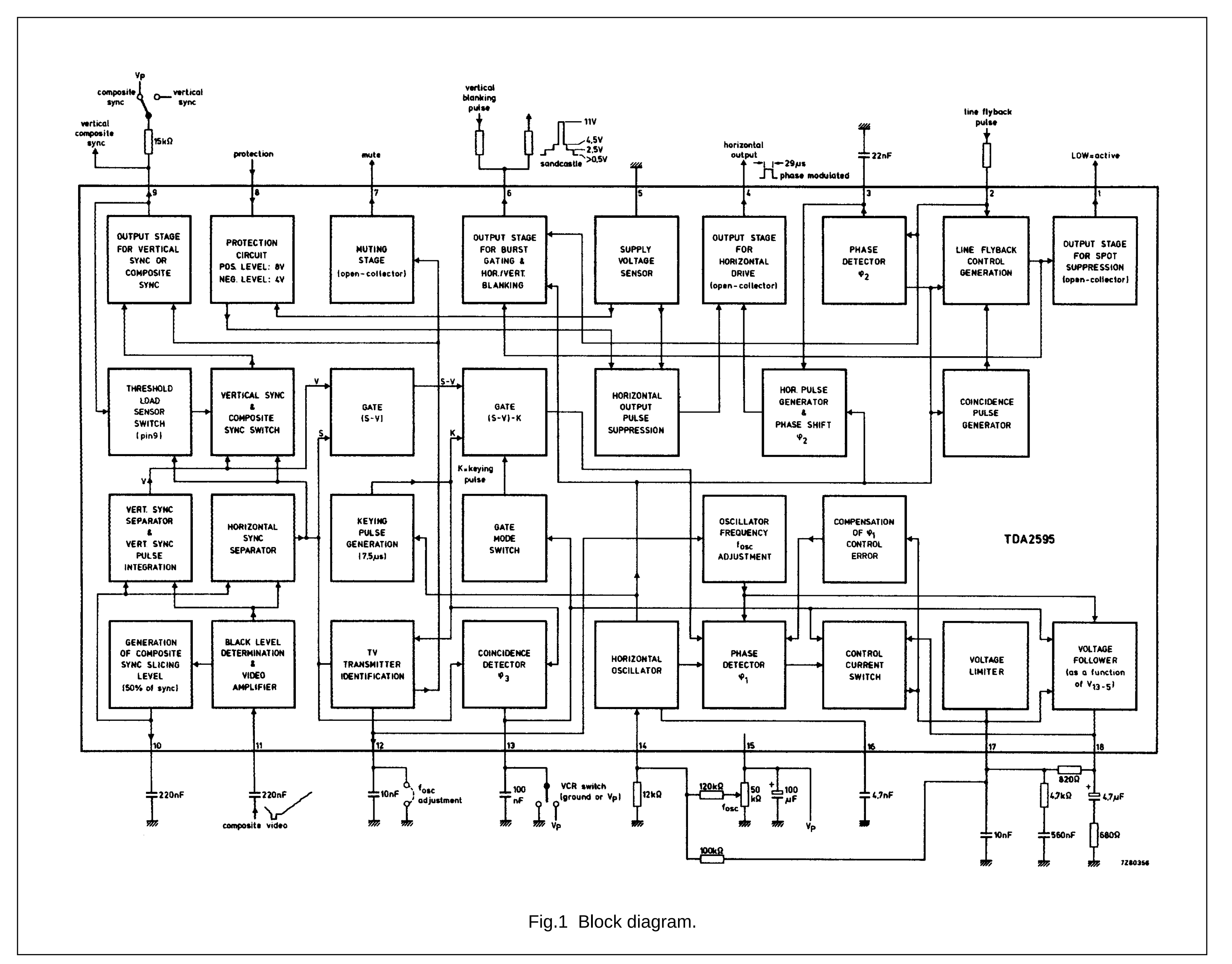


Fig.1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 15)	$V_{15\text{-}5} = V_P$	max.	13,2	V
Voltages at:				
pins 1, 4 and 7	$V_{1;4;7\text{-}5}$	max.	18	V
pins 8, 13 and 18	$V_{8;13;18\text{-}5}$	max.	V_P	V
pin 11 (range)	$V_{11\text{-}5}$	–0,5 to + 6		V
Currents at:				
pin 1	I_1	max.	10	mA
pin 2 (peak value)	$\pm I_{2M}$	max.	10	mA
pin 4	I_4	max.	100	mA
pin 6 (peak value)	$\pm I_{6M}$	max.	6	mA
pin 7	I_7	max.	10	mA
pin 8 (range)	I_8	–5 to +1		mA
pin 9 (range)	I_9	–10 to + 3		mA
pin 18	$\pm I_{18}$	max.	10	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}	–25 to + 125		°C
Operating ambient temperature range	T_{amb}	0 to + 70		°C

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; measured in Fig.1; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Composite video input and sync separator (pin 11)					
(internal black level determination)					
Input signal (positive video;					
standard signal; peak-to-peak value)	$V_{11\text{-}5(p\text{-}p)}$	0,2	1	3	V
Sync pulse amplitude					
(independent of video content)	$V_{11\text{-}5(p\text{-}p)}$	50	–	–	mV
Generator resistance	R_G	–	–	200	Ω
Input current during:					
video	I_{11}	–	5	–	μA
sync pulse	$-I_{11}$	–	40	–	μA
black level	$-I_{11}$	–	25	–	μA
Composite sync generation (pin 10)					
horizontal slicing level at 50% of the sync pulse amplitude for $V_{11\text{-}5(p\text{-}p)} < 1,5$ V					
Capacitor current during:					
video	I_{10}	–	16	–	μA
sync pulse	$-I_{10}$	–	170	–	μA
Vertical sync pulse generation					
slicing level at 30% (60% between black level and horizontal slicing level); pin 9					
Output voltage	$V_{9\text{-}5}$	10	–	–	V
Pulse duration	t_p	–	190	–	μs
Delay with respect to the vertical					
sync pulse (leading edge)	t_d	–	45	–	μs
Pulse-mode control					
output current for vertical sync pulse (dual integrated)		no current applied at pin 9			
output current for horizontal and vertical sync pulse (non-integrated separated signal)		current applied via a resistor of 15 kΩ from V_P to pin 9			

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Horizontal oscillator					
(pins 14 and 16)					
Frequency; free running	f_{osc}	–	15 625	–	Hz
Reference voltage for f_{osc}	V_{14-5}	–	6	–	V
Frequency control sensitivity	$\Delta f_{osc}/\Delta I_{14}$	–	31	–	Hz/μA
Adjustment range of circuit Fig.1	Δf_{osc}	–	± 10	–	%
Spread of frequency	Δf_{osc}	–	–	5	%
Frequency dependency (excluding tolerance of external (components)					
with supply voltage (V_P = 12 V)	$\frac{\Delta f_{osc}/f_{osc}}{\Delta V_{15-5}/V_{15-5}}$	–	± 0,05	–	
with supply voltage drop of 5 V	Δf_{osc}	–	–	10	%
with temperature	TC	–	–	$\pm 10^{-4}$	K^{-1}
Capacitor current during:					
discharging	$+ I_{16}$	–	1024	–	μA
charging	$- I_{16}$	–	313	–	μA
Sawtooth voltage timing (pin 14)					
rise time	t_r	–	49	–	μs
fall time	t_f	–	15	–	μs
Horizontal output pulse (pin 4)					
Output voltage LOW at I_4 = 50 mA	V_{4-5}	–	–	0,5	V
Pulse duration (HIGH)	t_p	–	29 ± 1,5	–	μs
Supply voltage for switching off the output pulse (pin 15)	V_P	–	4	–	V
Hysteresis for switching on the output pulse	ΔV_P	–	250	–	mV

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Phase comparison φ_1 (pin 17)					
Control voltage range	V_{17-5}	3,55	–	8,3	V
Leakage current					
at V_{17-5} = 3,55 to 8,3 V	I_{17}	–	–	1	μA
Control current for external					
time-constant switch	$\pm I_{17}$	1,8	2	2,2	mA
Control current at $V_{18-5} = V_{15-5}$					
and $V_{13-5} < 2$ V or $V_{13-5} > 9{,}5$ V	$\pm I_{17}$	–	8	–	mA
Control current at $V_{18-5} = V_{15-5}$					
and V_{13-5} = 2 to 9,5 V	$\pm I_{17}$	1,8	2	2,2	mA
Horizontal oscillator control					
control sensitivity	S_{φ}	6	–	–	kHz/μs
catching and holding range	$\pm\Delta f_{osc}$	–	680	–	Hz
spread of catching and holding range	$\pm\Delta f_{osc}$	–	10	–	%
Internal keying pulse					
at V_{13-5} = 2,9 to 9,5 V	t_p	–	7,5	–	μs
Time-constant switch					
slow time-constant at	V_{13-5}	9,5	–	2	V
fast time-constant at	V_{13-5}	2	–	9,5	V
Impedance converter offset voltage					
(slow time-constant)	$\pm V_{17-18}$	–	–	3	mV
Output resistance					
slow time-constant	R_{18-5}	–	–	10	Ω
fast time-constant	R_{18-5}	high impedance			
Leakage current	I_{18}	–	–	1	μA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Coincidence detector φ_3 (pin 13)					
Output voltage					
without coincidence with composite video signal	$V_{13\text{-}5}$	–	–	1	V
without coincidence without composite video signal (noise)	$V_{13\text{-}5}$	–	–	2	V
with coincidence with composite video signal	$V_{13\text{-}5}$	–	6	–	V
Output current					
without coincidence with composite video signal	I_{13}	–	50	–	µA
with coincidence with composite video signal	$-I_{13}$	–	300	–	µA
Switching current					
at $V_{13\text{-}5} = V_P - 0{,}5$ V	I_{13}	–	–	100	µA
at $V_{13\text{-}5} = 0{,}5$ V (average value)	$I_{13(av)}$	–	–	100	µA
Phase comparison φ_2 (pins 2 and 3) (see note 1)					
Input for line flyback pulse (pin 2)					
Switching level for φ_2 comparison					
and flyback control	$V_{2\text{-}5}$	–	3	–	V
Switching level for horizontal blanking	$V_{2\text{-}5}$	–	0,3	–	V
Input voltage limiting	$V_{2\text{-}5}$	–	–0,7	–	V
	or:	–	+4,5	–	V
Switching current					
at horizontal flyback	I_2	0,01	1	–	mA
at horizontal scan	I_2	–	–	2	µA
Maximum negative input current	$-I_2$	–	–	500	µA
Phase detector output (pin 3)					
Control current for φ_2	$\pm I_3$	–	1	–	mA
Control range	$\Delta t_{\varphi 2}$	–	19	–	µs
Static control error	$\Delta t / \Delta t_d$	–	–	0,2	%
Leakage current	I_3	–	–	5	µA

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Phase comparison φ_2 (pins 2 and 3) (continued)					
Phase relation between middle of the horizontal sync pulse and the middle of the line flyback pulse at t_{fp} = 12 µs (note 2)	Δt	–	2,6 ± 0,7	–	µs
If additional adjustment is required, it can be arranged by applying a current at pin 3	ΔI/Δt	–	30	–	µA/µs
Burst gating pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	10	11	–	V
Pulse duration	t_p	3,7	4	4,3	µs
Phase relation between middle of sync pulse at the input and the leading edge of the burst gating pulse at V_{6-5} = 7 V	$t_{\varphi 6}$	2,15	2,65	3,15	µs
Output trailing edge current	I_6	–	2	–	mA
Horizontal blanking pulse (pin 6) (note 3)					
Output voltage	V_{6-5}	4,1	4,5	4,9	V
Output trailing edge current	I_6	–	2	–	mA
Saturation voltage at horizontal scan	V_{6-5sat}	–	–	0,5	V
Clamping circuit for vertical blanking pulse (pin 6) (note 3)					
Output voltage at I_6 = 2,8 mA	V_{6-5}	2,15	2,5	3	V
Minimum output current at $V_{6-5} > 2,15$ V	I_{6min}	–	2,3	–	mA
Maximum output current at $V_{6-5} < 3$ V	I_{6max}	–	3,3	–	mA
TV-transmitter identification (pin 12) (note 4)					
Output voltage					
no TV transmitter	V_{12-5}	–	–	1	V
TV transmitter identified	V_{12-5}	7	–	–	V

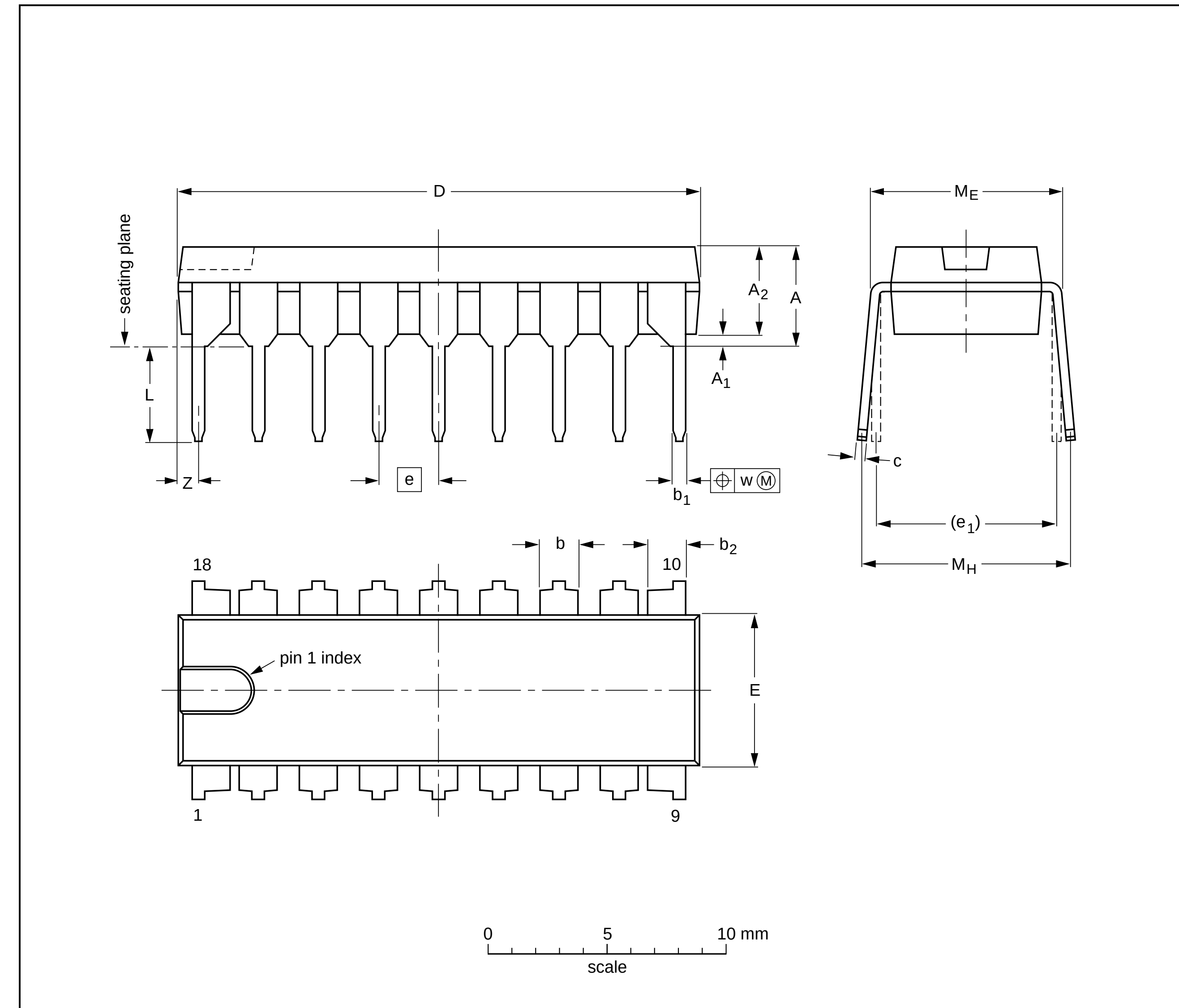
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Mute output (pin 7)					
Output voltage at I_7 = 3 mA no TV transmitter	V_{7-5}	–	–	0,5	V
Output resistance at I_7 = 3 mA no TV transmitter	R_{7-5}	–	–	100	Ω
Output leakage current at $V_{12-5} > 3$ V TV transmitter identified	I_7	–	–	5	µA
Protection circuit (beam-current/ EHT voltage protection) (pin 8)					
No-load voltage for $I_8 = 0$ (operative condition)	V_{8-5}	–	6	–	V
Threshold at positive-going voltage	V_{8-5}	–	8 ± 0,8	–	V
Threshold at negative-going voltage	V_{8-5}	–	4 ± 0,4	–	V
Current limiting for V_{8-5} = 1 to 8,5 V	$\pm I_8$	–	60	–	µA
Input resistance for $V_{8-5} > 8,5$ V	R_{8-5}	–	3	–	kΩ
Internal response delay of threshold switch	t_d	–	10	–	µs
Control output of line flyback pulse control (pin 1)					
Saturation voltage at standard operation; I_7 = 3 mA	V_{1-5sat}	–	–	0,5	V
Output leakage current in case of disturbance of line flyback pulse	I_1	–	–	5	µA

Notes to the characteristics

1. Phase comparison between horizontal oscillator and the line flyback pulse. Generation of a phase modulated (φ_2) horizontal output pulse with constant duration.
2. t_{fp} is the line flyback pulse duration.
3. Three-level sandcastle pulse.
4. If pin 12 is connected to V_p the vertical output is active independent of synchronization state.

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.